The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JOEL ZDEPSKI, RAMA KALLURI, HOWARD PAGE
and WOLF-HASSO KAUBISCH

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Appeal No. 1999-2306
Application 08/639,284

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ON BRIEF

_____

Before THOMAS, HAIRSTON and JERRY SMITH, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-28, which constitute all the claims in the application. An amendment after final rejection was filed on December 7, 1998, and was entered by the examiner.

The disclosed invention pertains to a method and apparatus for generating trickplay video streams, such as fast forward and fast reverse video streams, from a compressed normal play bitstream.

Representative claim 1 is reproduced as follows:

1. A computer-implemented method for generating trickplay streams from a compressed normal play bitstream, comprising:

receiving a compressed normal play bitstream, wherein said compressed normal play bitstream includes a plurality of intracoded frames and a plurality of intercoded frames;

extracting said intracoded frames from said compressed normal play bitstream, wherein said extracting includes storing said intracoded frames in a storage memory;

assembling said intracoded frames to form an assembled bitstream after said extracting;

decoding said assembled bitstream to produce a plurality of uncompressed frames; and

encoding said plurality of uncompressed frames after said decoding to produce a compressed trick play bitstream, wherein said compressed trick play bitstream includes only a subset of frames of said normal play bitstream.

The examiner relies on the following reference:

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| Lane et al. (Lane) | 5,623,344 | Apr. 22, 1997 (filed Aug. 19, 1994) |

Claims 1-28 stand rejected under 35 U.S.C. § 102(e) as being anticipated by the disclosure of Lane.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the disclosure of Lane fully meets the invention as set forth in claims 18, 20 and 21. We reach the opposite conclusion with respect to claims 1-17, 19 and 22-28. Accordingly, we affirm-in-part.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing

the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

The examiner indicates how he reads the claimed invention on the disclosure of Lane [answer, pages 4-7]. Appellants nominally argue the rejection against the claims in eight separate groupings [brief, page 3, reply brief, page 2].

Appellants' first grouping of claims includes claims 1, 2, 4, 5, 8-10, 12, 13, 16, 17, 25 and 26. With respect to these claims, appellants argue that Lane does not disclose generation of a trickplay stream at all. Appellants also argue that Lane does not disclose the step of extracting intracoded frames from the normal play bitstream which includes storing the intracoded frames in a storage memory. Appellants also argue that it is not clear that Lane forms an assembled bitstream from the extracted intracoded frames. Finally, appellants argue that Lane does not disclose decoding an assembled bitstream to produce uncompressed frames and then

encoding the uncompressed frames to produce a compressed trickplay bitstream as claimed [brief, pages 4-7].

The examiner responds that Lane teaches that D, I, B and P frames of video data are stored and processed. The examiner also responds that the assembled I-frames of video in Lane form an assembled bitstream as claimed. The examiner also responds that Lane teaches the decoding of received data packets and an encoder for producing a compressed trickplay bitstream as claimed [answer, pages 7-10]. Appellants respond that there is no disclosure in Lane that the extracted I-frames are stored. Appellants also respond that decoding packets of data is not the same as decoding a bitstream, and the decoding/encoding in Lane occur after the trickplay bitstream is formed rather than before as claimed [reply brief, pages 3-5].

With respect to the first group of claims, we agree with the position argued by appellants. We note that Lane appears to have two separate teachings which are relied on by the examiner. First, Lane describes a prior art fast play technique in which the I-frames of a sequence of a video bitstream are extracted and assembled in a sequence. Second,

Lane describes his own technique for fast play in which normal and trickplay segments of data are geometrically arranged on a videotape. The examiner refers to the prior art technique for meeting the extracting and assembling I-frames steps of the claimed invention but refers to Lane's technique for teaching the decoding and encoding of this assembled bitstream. In our view, these disparate teachings of Lane cannot be combined as proposed by the examiner to find anticipation.

With respect to the prior art technique disclosed by Lane, we agree with the examiner that this disclosure would have suggested to the artisan that a trickplay bitstream could be obtained by extracting I-frames from a normal play bitstream and assembling these I-frames in sequence. We also agree with the examiner that the disclosure in Lane would have suggested to the artisan that the extracted I-frames are stored. The person familiar with this art would have understood that bitstream frames in the prior art could be stored before they are processed. Lane's disclosure that the D-frames of MPEG compression are stored separately from the normal MPEG bitstream is sufficient to anticipate the storage of such frames as argued by the examiner. Lane, however,

teaches nothing about performing any further operations on the assembled I-frames. As noted above, the decoding and encoding steps of Lane which are relied on by the examiner have nothing to do with this prior art technique of assembling I-frames. The fact that encoding and decoding steps were known in a different embodiment does not anticipate applying these steps to the prior art embodiment of Lane.

Since we find that the decoding and encoding steps of Lane are not applicable to the prior art I-frames sequencing disclosed by Lane, we do not sustain the examiner's rejection of claims 1, 2, 4, 5, 8-10, 12, 13, 16, 17, 25 and 26. Since we have not sustained the rejection with respect to independent claims 1, 9, 17 and 26, we also do not sustain the anticipation rejection with respect to dependent claims 3, 6, 7, 11, 14, 15 and 27.

We now consider independent claim 18. Claim 18 is the same as claim 1 except that the final decoding and encoding steps are replaced by the step of storing the assembled bitstream. Appellants' only additional argument with respect to claim 18 is that Lane does not teach that the assembled bitstream is stored. As discussed above, however, we agree

with the examiner that Lane teaches that frames of a bitstream are stored. We find that this teaching extends to bitstreams which are in frame form such as D, I, B and P frames or frames which have been assembled in sequence such as the I-frames taught by Lane. The decoding and encoding steps of claim 1 which were found not anticipated by Lane are not present in claim 18. Thus, we agree with the examiner that the invention of claim 18 is fully met by the disclosure of Lane.

The fact that Lane indicates that the prior art technique would have difficult problems to overcome does not eliminate this disclosure as a valid reference. The prior art does not indicate that the problems cannot be solved, only that the problems are difficult to solve. Anticipation would not be defeated by merely arguing the level of difficulty involved unless it could be shown that the teaching relied on was not enabling. Such a showing is not present here. Therefore, we sustain the rejection of claim 18 and of claims 20 and 21 which are grouped therewith.

Claim 19, which depends from 18, is separately argued. Appellants argue that Lane relates to actions performed on packet headers rather than bitstream sequence headers as

claimed. The examiner disagrees with appellants and points to the operation of Lane's preferred embodiment.

As noted above, we find that Lane's preferred embodiment has nothing to do with the prior art embodiment also disclosed by Lane. Therefore, the headers of the data packets in Lane have nothing to do with bitstream sequence headers sent along with I-frames. The admitted prior art of Lane does not indicate how the I-frames are to be extracted from the normal bitstream or what specific information is to be extracted and assembled. Therefore, we agree with appellants that Lane does not disclose the extraction of sequence headers from a bitstream and the assembling of sequence headers along with the I-frames to form an assembled bitstream as recited in claim 19. Therefore, we do not sustain the examiner's rejection of claim 19.

Claims 22 and 23 are separately argued by appellants. These claims recite that matrices in the normal bitstream are located and included in the assembled bitstream. Appellants argue that there is no disclosure of matrices in Lane. The examiner responds that digitized video signals in the MPEG format are known to include matrices and the assembly of a

sequence of I-frames would include these matrices.

We agree with appellants. As noted above, Lane discloses nothing about how to extract the I-frames from the normal bitstream and how to assemble these I-frames in sequence. The admitted prior art in Lane does not indicate that matrices are to be located and assembled in forming the I-frames bitstream in the prior art. Therefore, we do not sustain the examiner's rejection of claims 22 and 23.

Claims 24 and 25 are separately argued by appellants. Since these claims include the decoding and encoding steps as discussed above with respect to claim 1, we do not sustain the examiner's rejection of claims 24 and 25.

Claim 28 is separately argued by appellants. Specifically, appellants argue that Lane does not disclose the recited use of a memory stack to store and retrieve markers and coordinates in response to finding start codes for data blocks, extension blocks and I-frame headers. The examiner finds that the steps of claim 28 are inherently performed in Lane. Appellants dispute this finding.

We agree with appellants. The disclosure of Lane does not support the examiner's findings of anticipation. Claim 28

recites a plurality of steps which are clearly not disclosed by Lane and cannot properly be considered to be inherently performed in Lane. Therefore, we do not sustain the examiner's rejection of claim 28.

In summary, we have sustained the examiner's anticipation rejection with respect to claims 18, 20 and 21, but we have not sustained the rejection with respect to each of the other claims on appeal. Therefore, the decision of the examiner rejecting claims 1-28 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

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| JAMES D. THOMAS<br>Administrative Patent Judge | ) |
| KENNETH W. HAIRSTON<br>Administrative Patent Judge | ) BOARD OF PATENT<br>) APPEALS AND<br>) INTERFERENCES |
| JERRY SMITH<br>Administrative Patent Judge | ) |

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JEFFREY C. HOOD
CONLEY ROSE & TAYON
P. O. BOX 3367
HOUSTON, TX 77253-3267

JS:caw